Amendments to the Claims:

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

1. (Currently Amended) A semiconductor circuit comprising:

a MOS transistor having:

spaced-apart source and drain regions of a first conductivity type that contact a semiconductor region of a second conductivity type, the semiconductor region having a top surface, one of the source and drain regions having a first bottom point that lies furthest away from the top surface, and a first depth measured from the top surface to the first bottom point along a line perpendicular to the top surface;

a channel region located between the source and drain regions; and

a gate formed over, and insulated from, the channel region; and

an imaging cell having:

spaced-apart source and drain regions of the first conductivity type that contact the semiconductor region, one of the source and drain regions of the imaging cell having a second bottom point that lies furthest away from the top surface, and a second depth measured from the top surface to the second bottom point along a line perpendicular to the top surface, wherein the second depth is substantially larger than the first depth;

a channel region located between the source and drain regions of the imaging cell; [[and]]

a floating gate formed over, and insulated from, the channel region of the imaging cell; and

a control gate well of the first conductivity type, the floating gate being formed over, and insulated from, the control gate well.

Claims 2-3. (Canceled)

4. (Currently Amended) The semiconductor circuit of ~~claim 2~~ claim 1 and further comprising a layer of oxide formed on the channel region of the imaging circuit and the control gate well, and under the floating gate.

5. (Original) The semiconductor circuit of claim 4 wherein the layer of oxide has a thickness that retains electrons for a period of time greater than six months.

6. (Original) The semiconductor circuit of claim 1 and further comprising a layer of oxide formed on the channel region of the imaging circuit and the control gate well, and under the floating gate, the layer of oxide having a thickness that retains electrons for a period of time that is greater than zero and less than three seconds.

7. (Original) The semiconductor circuit of claim 6 wherein the control gate well is formed in the semiconductor material.

8. (Original) The semiconductor circuit of claim 6 and further comprising an intermediate well that contacts the semiconductor material, the control gate well contacting the intermediate well, the intermediate well having an opposite conductivity type as the control gate well and the semiconductor material.

9. (Currently Amended) The semiconductor circuit of ~~claim 2~~ claim 1 wherein the control gate well contacts the semiconductor material.

10. (Currently Amended) The semiconductor circuit of ~~claim 2~~ claim 1 and further comprising an intermediate well that contacts the semiconductor material, the control gate well contacting the intermediate well, the intermediate well having an opposite conductivity type as the control gate well and the semiconductor material.

11. (Currently Amended) The semiconductor circuit of ~~claim 2~~ claim 1 and further comprising a control gate formed over, and insulated from, the floating gate.

Claims 12-20. (Canceled)